CLAIM AMENDMENTS

1. (Currently Amended) A method comprising:

amplifying data signals received from a memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

sampling the amplified data signals; and

selectively disabling the amplification in response to the absence of a predetermined operation occurring over the memory bus.

2. (Previously Presented) The method of claim 1, wherein the selectively disabling the amplification comprises:

selectively disabling sense amplifiers.

3. (Previously Presented) The method of claim 1, wherein the selectively disabling the amplification comprises:

selectively disabling the amplification in response to the end of a particular predetermined operation.

4. (Currently Amended) The method of claim 1, further comprising:

reading [[a]] said at least one data strobe signal from the bus;

delaying ~~the~~ said at least one data strobe signal; and

synchronizing the disabling of the amplification to ~~an edge~~ one or more of the one or more delayed data strobe ~~signal~~ signals.

5. (Original) The method of claim 1, further comprising:

communicating signals associated with a double data rate memory ~~device~~ bus over the memory bus.

6. (Original) The method of claim 1, wherein the predetermined operation comprises a read operation.

7. (Original) The method of claim 1, wherein the predetermined operation comprises a write operation.

8. (Currently Amended) A method comprising:

amplifying data signals received from a memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

sampling the amplified data signals; and

selectively enabling the amplification in response to a predetermined operation occurring over the memory bus.

9. (Previously Presented) The method of claim 8, wherein the selectively enabling the amplification comprises:

selectively enabling sense amplifiers.

10. (Previously Presented) The method of claim 8, wherein the selectively enabling the amplification comprises:

selectively enabling the amplification in response to the beginning of the predetermined operation.

11. (Currently Amended) The method of claim 8, further comprising:

synchronizing the enabling of the amplification ~~to the edge of a~~ of one or more edges of said at least one data strobe signal that appears on the memory bus in connection with the predetermined operation.

12. (Original) The method of claim 8, further comprising:

communicating signals associated with a double data rate memory ~~device~~ bus over the memory bus.

13. (Original) The method of claim 8, wherein the predetermined operation comprises a read operation.

14. (Original) The method of claim 8, wherein the predetermined operation comprises a write operation.

15. (Currently Amended) An apparatus comprising:

amplifiers to amplify data signals received from a memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

a first circuit coupled to the amplifiers to sample the amplified data signals; and

a second circuit to selectively disable the amplifiers in response to the absence of a predetermined operation occurring over the memory bus.

16. (Original) The apparatus of claim 15, wherein the second circuit selectively disables the amplifiers in response to the end of a particular read operation.

17. (Original) The apparatus of claim 15, wherein the predetermined operation comprises a read operation.

18. (Original) The apparatus of claim 15, wherein the predetermined operation comprises a write operation.

19. (Original) The apparatus of claim 15, wherein the apparatus comprises a memory controller.

20. (Original) The apparatus of claim 15, wherein the apparatus comprises a memory device.

21. (Currently Amended) An apparatus comprising:

amplifiers to amplify data signals received from a memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

a first circuit coupled to the amplifiers to sample the amplified data signals; and

a second circuit to selectively enable the amplifiers in response to a predetermined operation occurring over the memory bus.

22. (Original) The apparatus of claim 21, wherein the second circuit selectively disables the amplifiers in response to the end of a particular read operation.

23. (Original) The apparatus of claim 21, wherein the predetermined operation comprises a read operation.

24. (Original) The apparatus of claim 21, wherein the predetermined operation comprises a write operation.

25. (Original) The apparatus of claim 21, wherein the apparatus comprises a memory controller.

26. (Original) The apparatus of claim 21, wherein the apparatus comprises a memory device.

27. (Currently Amended) A computer system comprising:

a memory;

a memory bus coupled to the memory;

a processor to initiate a predetermined operation with the memory over the memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

amplifiers to amplify data signals received from the memory bus;

a first circuit coupled to the amplifiers to sample the amplified data signals; and

a second circuit to selectively disable the amplifiers in response to the absence of the predetermined operation occurring over the memory bus.

28. (Original) The computer system of claim 27, wherein the predetermined operation comprises one of a read operation and a write operation.

29. (Currently Amended) A computer system comprising:

a memory;

a memory bus coupled to the memory;

a processor to initiate a predetermined operation with the memory over the memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

amplifiers to amplify data signals received from the memory bus;

a first circuit coupled to the amplifiers to sample the amplified data signals; and

a second circuit to selectively enable the amplifiers in response to the predetermined operation occurring over the memory bus.

30. (Original) The computer system of claim 29, wherein the predetermined operation comprises one of a read operation and a write operation.

31. (New) A method comprising:

amplifying data signals received from a memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

sampling the amplified data signals; and

disabling the amplification in response to the absence of a predetermined operation occurring over the memory bus.

32. (New) The method of claim 31, wherein the disabling the amplification comprises:

selectively disabling sense amplifiers.

33. (New) The method of claim 31, wherein the disabling the amplification comprises:

selectively disabling the amplification in response to the end of a particular predetermined operation.

34. (New) A method comprising:

amplifying data signals received from a memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

sampling the amplified data signals; and

enabling the amplification in response to a predetermined operation occurring over the memory bus.

35. (New) The method of claim 34, wherein the enabling the amplification comprises:

selectively enabling sense amplifiers.

36. (New) The method of claim 34, wherein the enabling the amplification comprises:

selectively enabling the amplification in response to the beginning of the predetermined operation.

37. (New) An apparatus comprising:

amplifiers to amplify data signals received from a memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

a first circuit coupled to the amplifiers to sample the amplified data signals; and

a second circuit to disable the amplifiers in response to the absence of a predetermined operation occurring over the memory bus.

38. (New) The apparatus of claim 37, wherein the second circuit disables the amplifiers in response to the end of a particular read operation.

39. (New) The apparatus of claim 37, wherein the predetermined operation comprises a write operation.

40. (New) An apparatus comprising:

amplifiers to amplify data signals received from a memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

a first circuit coupled to the amplifiers to sample the amplified data signals; and

a second circuit to enable the amplifiers in response to a predetermined operation occurring over the memory bus.

41. (Original) The apparatus of claim 40, wherein the predetermined operation comprises a read operation.

42. (New) The apparatus of claim 21, wherein the predetermined operation comprises a write operation.